What is claimed is:

1. A microcomputer for performing information processing, comprising:

a processor for executing instructions;

an external bus being connectable to an emulation memory and at least one external memory other than said emulation memory; and

bus control means for connecting a bus of said processor to said external bus so that an access of said processor to an internal memory will be switched to an access to said emulation memory through said external bus when said microcomputer is in an emulation mode.

2. The microcomputer according to claim 1, further comprising a mode selection terminal for selecting ON or OFF of the emulation mode.

3. The microcomputer according to claim 1, further comprising a mode selection register for storing information used to select ON or OFF of the emulation mode, and being accessible by said processor.

4. The microcomputer according to claim 1,

wherein an address bus of said processor is connected to an external address bus and an address bus of said internal memory without dependent on ON/OFF of the emulation mode, and

wherein a data bus of said processor is connected to an external data bus when the emulation mode becomes ON.

5. The microcomputer according to claim 1, further comprising memory control means for outputting a first control signal for controlling said external memory connected to said external bus and a second control signal for controlling said emulation memory connected to said external bus, said second control signal being different from said first control signal.

6. The microcomputer according to claim 5,

wherein said second control signal includes a second memory read signal which becomes active at a timing earlier than that of a first memory read signal included in said first control signal.

7. The microcomputer according to claim 1, further comprising a mode selection terminal for selecting a first mode and a second mode, said emulation memory being first accessed by said processor after reset in said first mode, and said internal memory being first accessed by said processor after reset in said second mode.

8. The microcomputer according to claim 7,

wherein said mode selection terminal is capable of selecting a third mode in which said external memory is first accessed by said processor after reset.

9. The microcomputer according to claim 7,

wherein said mode selection terminal is capable of selecting a fourth mode in which information is transmitted from said external memory to said emulation memory after reset and thereafter said emulation memory is first accessed by said processor.

10. Electronic equipment comprising:

the microcomputer as defined in claim 1;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

11. Electronic equipment comprising:

the microcomputer as defined in claim 2;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

12. Electronic equipment comprising:

the microcomputer as defined in claim 3;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed

by said microcomputer.

13. Electronic equipment comprising:

the microcomputer as defined in claim 4;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

14. Electronic equipment comprising:

the microcomputer as defined in claim 5;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

15. Electronic equipment comprising:

the microcomputer as defined in claim 6;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

16. Electronic equipment comprising:

the microcomputer as defined in claim 7;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomput r.

17. Electronic equipment comprising:

the microcomputer as defined in claim 8;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

18. Electronic equipment comprising:

the microcomputer as defined in claim 9;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

19. An emulation method for a microcomputer comprising a processor for executing instructions, and an external bus being connectable to an emulation memory and at least one external memory other than said emulation memory,

wherein said external bus is shared between said emulation memory and said external memory and said emulation memory is accessed through said external bus when the microcomputer is on evaluation, thereby causing said processor to operate according to information read out from said emulation memory, and

wherein said processor is operat d according to information read out from said internal memory when th microcomputer is on production.

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